Appl. No. 10/613,175

Examiner: SMOOT, STEPHEN W, Art Unit 2813

In response to the Office Action dated October 14, 2004

Date: December 21, 2004 Attorney Docket No. 10112431

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (original): A test device for detecting alignment of deep trench capacitors and word lines in DRAM devices with vertical transistors, wherein the test device is disposed in a scribe line region of a wafer, comprising:

an active area disposed in the scribe line region;

an H-type deep trench capacitor disposed in the active area, having parallel first and second portions and a third portion, wherein each of the first and second portions has a center and two ends, and the third portion is disposed between the centers of the first and second portions;

first to fourth conductive pads disposed on the two ends of the first and second portions respectively; and

a bar-type conductive pad disposed between the first and second portions, having a center aligned with a center of the third portion.

Claim 2 (original): The test device as claimed in claim 1, wherein the first to fourth conductive pads and the bar-type conductive pad are made of the same material.

Claim 3 (original): The test device as claimed in claim 1, wherein the first to fourth conductive pads and the bar-type conductive pad are made of polysilicon.

Claim 4 (original): The test device as claimed in claim 1, wherein the bar-type conductive pad, the first portion and the second portion are parallel.

Claim 5 (currently amended): A method for detecting alignment of deep trench capacitors and word lines in DRAM devices with vertical transistors, comprising:

providing a wafer with at least one scribe line region and at least one memory region; forming a plurality of memory cells with vertical transistors in the memory region and at least one test device in the scribe line <u>region</u> simultaneously, wherein the

Appl. No. 10/613,175 Date: December 21, 2004 Examiner: SMOOT, STEPHEN W, Art Unit 2813 Attorney Docket No. 10112431

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memory cells have word line areas and deep trench capacitors, the test device including:

an active area disposed in the scribe line region;

an H-type deep trench capacitor disposed in the active area, having parallel first and second portions and a third portion, wherein each of the first and second portions has a center and two ends, and the third portion is disposed between the centers of the first and second portions;

first to fourth conductive pads disposed on the two ends of the first and second portions respectively; and

a bar-type conductive pad disposed between the first and second portions, having a center aligned with a center of the third portion;

detecting a first resistance between the first conductive pad disposed on the first portion and the bar-type conductive pad, and a second resistance between the second conductive pad disposed on the second portion and the bar-type conductive pad:

determining alignment of the H-type deep trench capacitor and the bar-type conductive pad according to the first resistance and the second resistance; and

determining alignment of the deep trench capacitors and word lines in the memory regions region according to alignment of the H-type deep trench capacitor and the bar-type conductive pad of the test device.

Claim 6 (original): The method as claimed in claim 5, wherein the bar-type conductive pad is a predetermined distance from the first and second portions.

Claim 7 (currently amended): The method as claimed in Claim 6, further comprising a step of determining alignment shift (ΔL) of the H-type deep trench capacitor and the bar-type conductive pad area according to the first resistance, the second resistance, and the predetermined distance between first and second portions and the bar-type conductive pad respectively.

Claim 8 (original): The method as claimed in Claim 7, wherein the alignment shift (ΔL) is determined by an equation:

$$\Delta L = L \times \frac{(R2-R1)}{(R2+R1)}\,;$$

Appl. No. 10/613,175

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wherein L is the predetermined distance between first and second portions and the bartype conductive pad respectively; R1 is the first resistance between the first
conductive pad disposed on the first portion and the bar-type conductive pad;
and R2 is the second resistance between the second conductive pad disposed
on the second portion and the bar-type conductive pad.

Claim 9 (original): The method as claimed in claim 5, wherein the first to fourth conductive pads and the bar-type conductive pad are made by the same material.

Claim 10 (original): The method as claimed in claim 5, wherein the first to fourth conductive pads and the bar-type conductive pad are made of polysilicon.

Claim 11 (original): The method as claimed in claim 5, wherein the bar-type conductive pad, the first portion and the second portion are parallel.

Claim 12 (currently amended): The method as claimed in claim 5, wherein the alignment of the H-type trench eapacitors capacitor and the bar-type conductive pad is abnormal when the first resistance does not equal the second resistance.